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Design and Schematic-Level Verification of a Multi-Mode Low-Drift RC Oscillator for DC-DC Converters

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Abstract: This paper presents a multi-mode RC relaxation oscillator intended for clock generation in DC-DC converters. The architecture combines a supply-rejection-enhanced voltage reference, a compensated low-dropout regulator, a low-drift bias network, bidirectional current trimming, mode decoding, and an alternating-capacitor timing core. It supports two fixed-frequency modes, resistor-programmed operation from 100 to 800 kHz, and an external-clock interface. The circuit was designed in a CSMC 0.18-µm 1P6M CMOS process and evaluated by schematic-level Cadence Spectre simulations. The reference exhibits a simulated temperature coefficient of 15.67 ppm/°C and a low-frequency power-supply rejection of 93 dB. The local regulator achieves a 62.492° phase margin, 0.225 mV/mA load regulation, and 0.166%/V line regulation. The oscillator frequency span is 0.3125% over the documented 3.6-6.0 V sweep and 0.28575% over the documented -40 to 125 °C sweep. Nominal subsystem power is 532 µW at 500 kHz, 5 V, TT, and 25 °C. Device dimensions, component values, and complete transistor connectivity are intentionally omitted.

Keywords: RC oscillator; DC-DC converter; Multi-mode clock; Low-drift bias; Power-supply rejection; CMOS.

1. Introduction

The switching frequency is a central design variable in a DC-DC converter because it fixes the timing of power-stage commutation, influences the energy transferred in each cycle, and sets the frequency range over which control-loop filtering and electromagnetic-interference mitigation must operate. An inaccurate or supply-sensitive internal clock changes ripple, peak current, duty-ratio limits, and light-load behavior even when the power-stage devices and feedback controller are unchanged. A converter therefore benefits from an integrated oscillator that is stable across the input-voltage and temperature ranges while retaining enough programmability to support different inductors, loads, and operating modes.

On-chip RC oscillators are attractive in power-management integrated circuits because they avoid crystals and large off-chip timing components. Their accuracy, however, is limited by resistor and capacitor process spread, comparator delay, supply-dependent thresholds, and temperature-sensitive bias current. Recent measured oscillators have addressed these errors with self-threshold tracking, frequency-locked loops, pulse-density-modulated resistors, multi-point trimming, and ratiometric references [2-7]. Those approaches demonstrate excellent energy efficiency or parts-per-million stability, but they frequently optimize a single nominal frequency and a narrow supply domain. A DC-DC controller has a different integration problem: the timing generator must coexist with a wide input supply, local regulation, mode decoding, trimming, ramp generation, and protection circuitry.

This work develops a functionally integrated solution for that use case. The proposed architecture combines a reference with local power-supply-rejection feedback, a compensated low-dropout regulator (LDO), a low-drift bias network, two-direction current trimming, a mode-selection network, and an alternating-capacitor relaxation core. The mode interface provides nominal 250- and 500-kHz outputs, resistor-programmed operation over 100-800 kHz, and an external-clock path. The design objective is not to claim a state-of-the-art standalone timer. Instead, it is to reduce the interaction between the wide input supply and the timing core while giving a DC-DC system several practical frequency-control options in one 0.18-µm CMOS implementation.

All results reported here were obtained from schematic-level Cadence Spectre simulations; no silicon measurements or extracted-layout simulations are claimed. The principal contributions are: (1) a wide-input local-regulation chain that attenuates supply coupling before it reaches the timing core; (2) a multi-mode current-steering interface supporting fixed, resistor-programmed, and external-clock operation; and (3) a bidirectional trim architecture combined with an alternating timing core. Function-level diagrams are used to protect proprietary device dimensions and complete transistor connectivity.

2. Design Objectives and System Architecture

2.1. Functional Requirements

The oscillator was developed for a converter input domain of 3.5-6.0 V and a design temperature range of -55 to 125 °C. A local regulated supply isolates the timing path from the wide input node. The frequency interface is required to support two internally selected fixed settings, an externally programmed resistance, and a synchronization input. A separate ramp signal is generated for the pulse-width-modulation path. Frequency accuracy must therefore be considered together with reference stability, LDO loop stability, bias-current drift, switching delay, and the digital-to-analog boundary of the mode-control network.

A hierarchical design strategy was adopted. Supply disturbances are first attenuated in the reference and local regulator; the resulting regulated voltage is converted into bias currents; trimming compensates process-induced error in the charging current; and mode logic selects the current applied to the timing capacitors. This ordering avoids asking the timing core alone to reject every supply and process perturbation. It also allows each supporting block to be

verified by a metric that can be traced to oscillator behavior, such as reference temperature coefficient, reference and LDO PSR, LDO phase margin, and current-selection state.

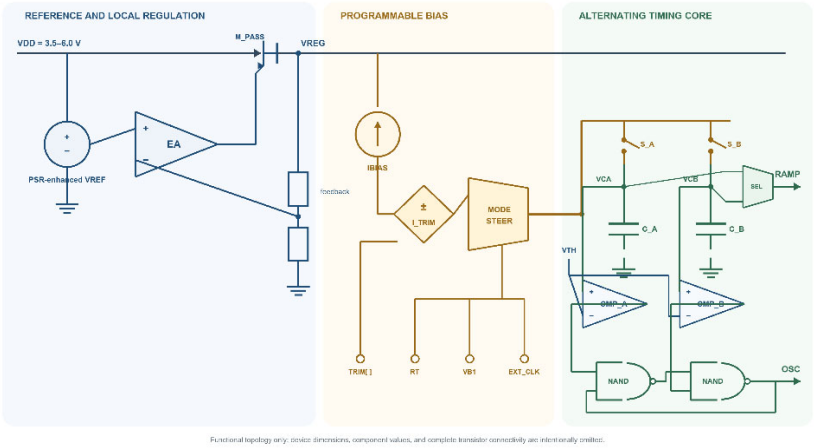


Fig. 1 Circuit-topology-level representation of the regulated reference, programmable bias, and alternating timing paths; device values and complete transistor connectivity are omitted.

2.2. Timing Principle

The timing core uses controlled charging and rapid reset of alternating capacitor nodes. During one half-cycle, the selected bias current charges the active node toward an upper comparison threshold. The corresponding comparator changes state when the threshold is crossed, the latch toggles, and the node is discharged while the complementary node begins its charging interval. Alternation prevents a single node from carrying the entire reset and charge history and provides a convenient path for generating both the clock and a ramp-related signal. In first order, frequency increases with charging current and decreases with the effective timing capacitance and threshold swing; comparator and latch delay add a secondary period error.

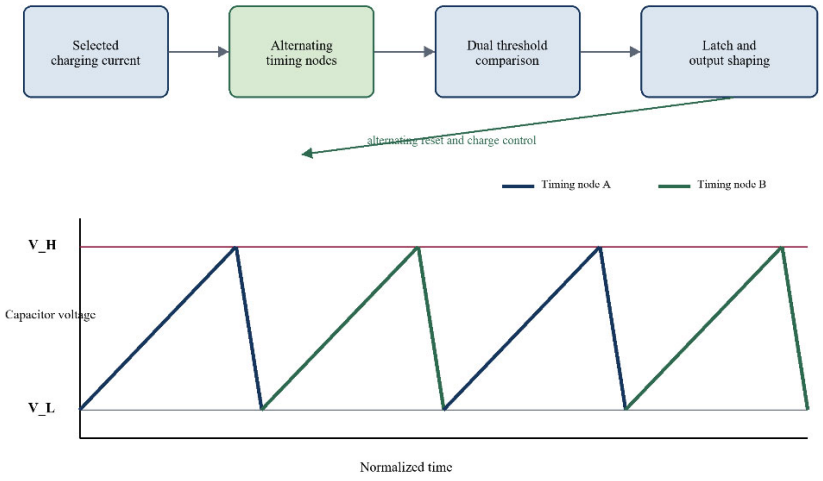


Fig. 2 Simplified timing sequence and normalized alternating-node waveforms; device sizes and capacitor values are omitted.

Table 1. Functional mode map used in circuit simulation.

Operating mode	VB1 condition	RT condition	Selected charging path
Fixed 250 kHz	Low	Open	Iref_A disabled; Iref_B selected
Fixed 500 kHz	High	Open	Iref_A and Iref_B selected
Resistor programmed	High impedance	50-250 kΩ	External-resistance-controlled path
External-clock interface	Clock applied	Mode-setting resistance	Synchronization control path

The design therefore controls frequency primarily through current selection rather than by exposing internal capacitor values. The fixed modes use predefined current combinations, the resistor-programmed mode maps the RT pin to a charging-current condition, and the external-clock path changes the mode-control state so that the internal oscillator can interact with the applied timing signal. The available external-clock waveform demonstrates that the path is activated, but it does not provide lock-acquisition time, phase error, or jitter. Consequently, this paper treats external synchronization as a

functional interface and does not claim a measured phase-locked result.

2.3. Frequency Model and First-Order Sensitivity

Let V1 denote the regulated bias-setting voltage, RO the effective bias resistance, Ceff the effective timing capacitance, and ΔV the comparator threshold swing. The charging current and the corresponding first-order charging interval are

$$I_s = \frac{V_1}{R_O} \quad (1)$$

$$t_{ch} = \frac{C_{eff}\,\Delta V}{I_{ch}} \quad (2)$$

For approximately symmetric half-cycles, the period contains two charging/reset intervals and the aggregate comparator-latch delay td. A compact timing model is therefore

$$T \approx 2t_{ch} + 2t_{dis} + 2t_d, \; f = \frac{1}{T} \quad (3)$$

When the charging term dominates the period, linearization gives the following first-order fractional sensitivity. The final term identifies why comparator and latch delay become increasingly important at the upper end of the tuning range.

$$\frac{\delta f}{f} \approx \frac{\delta I_{ch}}{I_{ch}} - \frac{\delta C_{eff}}{C_{eff}} - \frac{\delta \Delta V}{\Delta V} - \frac{2\delta t_d}{T} \quad (4)$$

Equations (1)-(4) connect the circuit hierarchy to frequency accuracy without revealing device sizes or timing-component values. Reference and LDO rejection reduce variations in V1 and ΔV, the bias and trim network controls Ich, matched alternating paths limit differential changes in Ceff and threshold swing, and balanced comparison paths reduce delay asymmetry. The model also explains why the reported supply and temperature sweeps characterize the integrated signal chain rather than the timing capacitor alone.

3. Circuit Design

3.1. Reference and Local Regulation

The voltage reference combines devices with complementary threshold-voltage temperature behavior and a local negative-feedback path. The feedback senses supply-induced movement in an internal node and applies an opposing change to the reference branch. This function-level arrangement is consistent with the broader requirement that a reference used inside a switching converter must reject both low-frequency supply variation and switching-related perturbations [1, 8]. The reference is not presented as an isolated precision source; it is designed as the first stage in a chain that ultimately stabilizes the timing current.

The LDO receives the wide input supply and produces the internal regulated domain used by the bias and oscillator blocks. Its loop contains an error amplifier, buffer, pass path, and resistive feedback. A dynamic zero-compensation branch is connected to an internal high-impedance node so that the loop zero offsets the non-dominant pole over the intended load range. This choice is important because an underdamped local regulator can convert oscillator current steps into supply ringing, while an excessively narrow loop can allow low-frequency supply movement to modulate the threshold and charging current. The design therefore evaluates load regulation, line regulation, phase margin, and PSR rather than relying on a DC output value alone.

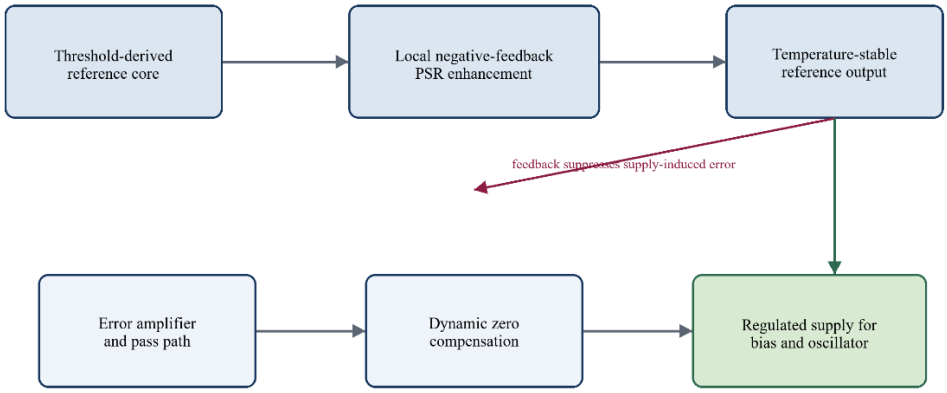


Fig. 3 Function-level view of the reference feedback and the compensated local regulator.

3.2. Bias and Bidirectional Trimming

A temperature-stable bias current is generated from the reference voltage and a resistor selected for low net drift. Cascoded current mirrors distribute scaled copies to the comparators, amplifiers, trimming network, and timing branches. The current mirrors are arranged so that the oscillator receives separate charging controls for the alternating timing paths. The architecture allows the mode-control block to change frequency without reconfiguring the reference or regulator, reducing transients at shared analog nodes.

Process compensation is provided by a segmented current-trim network. One trim direction injects binary-weighted current into the bias path, while the other reduces the effective branch current through a programmable resistive element. The two directions are valuable because a one-sided trim can correct only one sign of process error and may force the nominal design away from its optimal operating point. The reported work does not include a Monte Carlo distribution, so the trim range is documented as an architectural provision rather than a statistically verified yield result.

3.3. Mode Decoder and Relaxation Core

The VB1 and RT interface is translated into complementary selection signals that steer the bias currents. In the low fixed-frequency state, one charging branch is disabled and the other remains active. In the high fixed-frequency state, both branches contribute. With VB1 held in a high-impedance condition, the RT resistance controls the programmable charging path and supports the 100-800-kHz operating range. Input filtering and level interpretation are included so that pin noise does not directly toggle the analog current mirrors.

The core contains two comparison paths, alternating timing nodes, a reset network, and latch-based output control. Matching between the comparator inputs and symmetry

between the alternating timing branches are more important than absolute device size for first-order accuracy. The functional description therefore focuses on balanced comparison and charging paths while omitting complete transistor connectivity, device dimensions, and timing-capacitor values.

3.4. Error Pathways and Design Mitigation

The oscillator period can be viewed as the sum of a current-controlled charging interval and a finite switching delay. Supply movement can perturb the period through the reference voltage, the regulated rail, the mirror output resistance, the comparator threshold, and the latch delay. The design attenuates these pathways in sequence: local feedback first stabilizes the reference, the LDO isolates the analog domain, cascoded mirrors reduce current modulation, and symmetric timing branches limit differential disturbance. This layered approach is more appropriate for a wide-input power-management circuit than assigning the entire rejection requirement to one high-gain node.

Table 2. Dominant error pathways, mitigation, and available evidence.

Error pathway	Primary circuit effect	Design mitigation	Evidence boundary
Input-supply variation	Reference and bias-current modulation	Reference feedback plus local LDO isolation	DC and AC schematic simulation
Temperature	Reference, resistance, mirror, and delay drift	Complementary drift and matched distribution	Reference and oscillator sweeps
Global process variation	Charging-current and timing-constant shift	Bidirectional segmented trim	Architecture shown; yield not quantified
Local mismatch	Half-cycle and threshold asymmetry	Balanced comparison and charging paths	No Monte Carlo data
Switching coupling	Clock-edge injection into analog nodes	Analog-node isolation and filtered controls	Schematic-level risk analysis
Mode transitions	Momentary current-selection disturbance	Complementary decoding and analog-node isolation	Settled modes verified; transition metrics pending

Temperature affects the reference, the resistance used to establish the bias current, current-mirror ratios, comparator overdrive, and parasitic delay. The reference and resistor are selected so that their dominant temperature tendencies partially cancel in the bias path. Residual error is then reduced by using the same regulated domain and closely matched current-transfer structures for both half-cycles. Because the documented oscillator sweep is not demonstrably linear, the resulting frequency behavior is evaluated by its total span rather than by fitting a single temperature coefficient.

Process variation changes absolute resistance, capacitance, threshold voltage, and device transconductance. The bidirectional trim network addresses the resulting charging-current offset without requiring disclosure of device dimensions or capacitor values. It does not remove mismatch between nominally equal devices. For that reason, trim is treated as a calibration mechanism, while mismatch-aware design and later Monte Carlo verification remain separate requirements.

Mode changes introduce a further dynamic error source. A digital selection edge can couple charge into a bias node or momentarily enable incompatible current paths. The decoder therefore generates complementary analog control states and isolates the timing core from direct pin transitions. Verification of a mode is based on the selected current state and the settled clock waveform; the available dataset does not establish glitch energy, transition latency, or uninterrupted phase continuity during an in-cycle mode change.

4. Simulation and Verification Methodology

4.1. Process and Analysis Conditions

The circuit was implemented with the CSMC 0.18-μm 1P6M CMOS design kit and simulated in Cadence Spectre. Unless a sweep is stated explicitly, nominal functional waveforms use the TT process condition, VDD = 5 V, and 25 °C. The reference temperature sweep covers -55 to 125 °C. The oscillator frequency-versus-temperature dataset documented in the source material covers -40 to 125 °C; the wider -55 to 125 °C value is retained only as the intended design range. Likewise, the overall input specification is 3.5-6.0 V, whereas the detailed oscillator frequency sweep begins at 3.6 V. This separation between design range and documented sweep range avoids extrapolating beyond the available data.

Table 3. Simulation matrix and interpretation boundaries.

Block or function	Analysis	Documented condition	Reported quantity
Reference	Temperature DC	5 V; -55 to 125 °C; TT	15.67 ppm/°C
Reference	AC PSR	Small-signal supply injection	93 dB at low frequency
LDO	Load DC	1 nA to 20 mA	0.225 mV/mA
LDO	Line DC	3.6 to 6.0 V	0.166%/V
LDO	STB	Full-load loop	62.492° phase margin
Oscillator	Transient	TT; 5 V; 25 °C	Mode functionality
Oscillator	Supply sweep	3.6 to 6.0 V	0.3125% span
Oscillator	Temperature sweep	-40 to 125 °C	0.28575% span

DC analyses were used for reference drift, LDO line regulation, load regulation, and overtemperature thresholds. AC analysis determined reference and regulator PSR. A loop-stability testbench provided the LDO loop gain and phase margin. Transient simulations verified the 250-kHz, 500-kHz,

resistor-programmed, and external-clock modes. Frequency robustness was then evaluated by sweeping supply voltage and temperature. Average power was calculated at the nominal 500-kHz operating point. The available dataset does not contain process-corner tables, Monte Carlo mismatch, startup statistics, cycle-to-cycle jitter, phase noise, or extracted-layout simulations; these quantities are therefore not inferred.

4.2. Acceptance Criteria and Reproducibility

Each functional result was accepted only when the stimulus, observed node, operating condition, and reported metric could be associated with a named block or mode. For fixed-frequency and resistor-programmed operation, this requires both a stable periodic output and current-selection behavior consistent with Table 1. For support blocks, a DC output value alone is insufficient: temperature drift, line or load dependence, loop stability, and supply rejection are examined because each quantity represents a separate route by which the oscillator period can move.

The numerical values reported in this paper are taken from the documented schematic-level plots and calculation records. Percent spans are retained in the form supported by those records, and no additional precision is inferred from the raster plots. The 3.5-V lower limit and -55 °C lower temperature limit are design targets, whereas the available oscillator sweep evidence begins at 3.6 V and -40 °C. Repeating that distinction in tables and captions prevents the specification limits from being mistaken for characterized endpoints.

A reproducible extension of the work should use the same hierarchy of testbenches. The reference and regulator should first be checked independently, followed by bias and trim-code sweeps, individual oscillator modes, and finally the integrated subsystem. Corner and mismatch runs should record frequency, duty ratio, startup time, current consumption, and regulator stability with explicit simulator tolerances and extraction status. This order helps identify whether a failed frequency point originates in the timing core or in the supporting analog supply chain.

5. Results

5.1. Reference and Regulator

At 5 V and TT, the reference output is approximately 0.973 V. The -55 to 125 °C sweep yields a simulated temperature coefficient of 15.67 ppm/°C. The low-frequency PSR is approximately 93 dB and decreases toward about 30 dB at high frequency. These results indicate that the feedback path reduces slow supply-induced movement at the reference node, while the high-frequency behavior remains limited by device and node capacitances. For a switching-converter application, the low-frequency result supports input-line rejection, whereas the reduced high-frequency rejection reinforces the need for local regulation and careful routing around the switching edges.

The LDO output changes by about 4.5 mV when the load is swept from 1 nA to 20 mA, corresponding to 0.225 mV/mA. Its output changes by approximately 3.99 mV for an input sweep from 3.6 to 6.0 V, reported as 0.166%/V line regulation. The full-load loop has a 62.492° phase margin. Simulated PSR is about 70 dB at 1 Hz and 46.531 dB at 10 kHz. Taken together, the phase-margin and PSR results support the use of the regulator as an isolation stage between the wide input rail and the timing core, although load-transient settling and extracted parasitics remain to be evaluated.

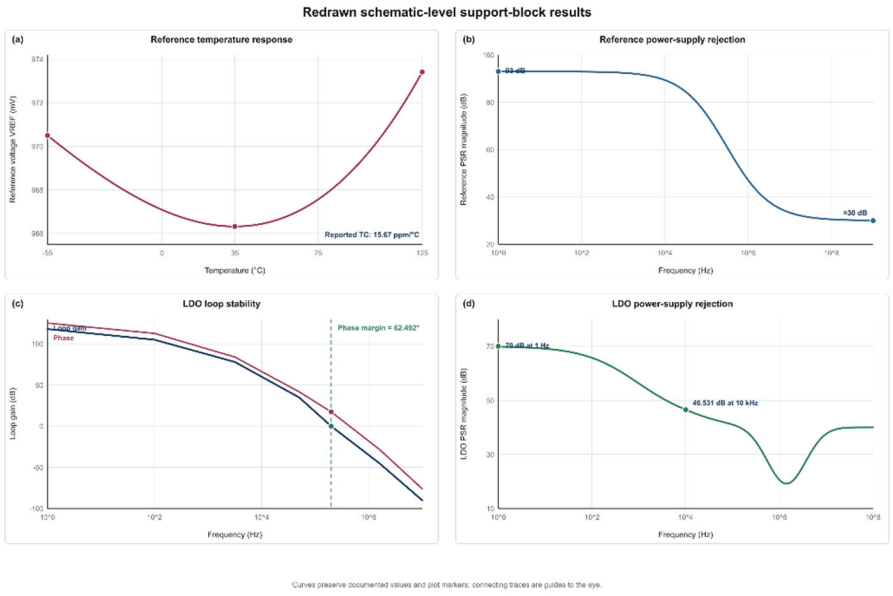


Fig. 4 Redrawn schematic-level support-block results: (a) reference temperature response, (b) reference power-supply rejection, (c) LDO loop stability, and (d) LDO power-supply rejection. Curves preserve the documented values and markers; connecting traces are guides to the eye.

5.2. Frequency Modes

Transient analysis confirms the two fixed-frequency states. With the low fixed-mode condition applied, the output is nominally 250 kHz; with the high fixed-mode condition, it is nominally 500 kHz. The current-selection waveforms show that the intended charging branches are enabled in each state. In resistor-programmed operation, an RT value of 100 kΩ produces an output close to 450 kHz under the nominal simulation condition, consistent with the stated 100-800-kHz tuning range for the wider resistance interval.

The external-clock case shows switching of the synchronization control path and a corresponding oscillator response. The recorded output is approximately 230 kHz for the documented test configuration. Because the available evidence does not show equality between the applied clock

and output frequency, phase convergence, or a lock detector, the waveform is not used to claim one-to-one synchronization accuracy. It is instead treated as evidence that the external-clock mode changes the internal timing state without disrupting oscillation. The present schematic-level dataset does not quantify lock range, acquisition time, or phase error; those metrics require a dedicated synchronization testbench.

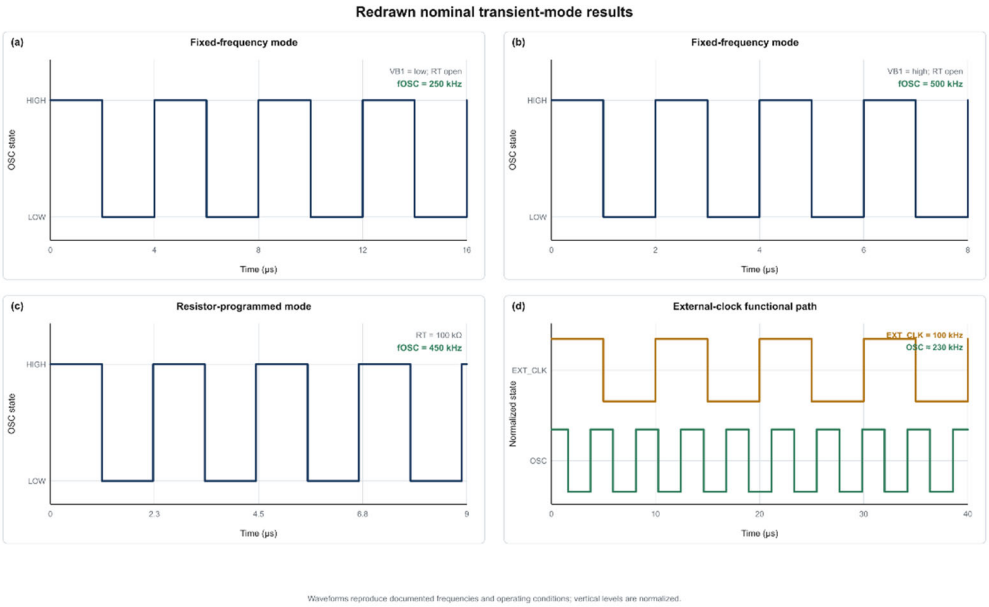


Fig. 5 Redrawn nominal transient results for (a) 250-kHz fixed mode, (b) 500-kHz fixed mode, (c) resistor-programmed operation, and (d) the external-clock functional path. Waveforms reproduce the documented frequencies and operating conditions; vertical levels are normalized.

5.3. Supply Temperature and Power

When the supply is swept from 3.6 to 6.0 V, the simulated oscillator frequency remains between 413.28 and 414.53 kHz for the selected programmable-mode condition. The 1.25-kHz span corresponds to 0.3125%. This result reflects the combined action of the reference, local regulator, and bias-current path; it should not be attributed to the timing core alone. The direction of the small change is less important than the bounded span because multiple device effects contribute across the wide-input range.

For the documented -40 to 125 °C oscillator sweep, the reported maximum frequency change is 1.143 kHz, or 0.28575% relative variation. The result is consistent with a charging current that remains nearly temperature independent after reference and resistor compensation. It is reported as total variation rather than converted into a parts-per-million-per-degree coefficient because the available data do not establish a linear temperature dependence or provide the underlying numerical samples. At 500 kHz, 5 V, TT, and 25 °C, the complete oscillator subsystem consumes 532 µW. This power includes support circuitry and is therefore higher than that of specialized low-voltage wake-up timers.

Table 4. Consolidated simulated performance of the proposed oscillator subsystem.

Category	Metric	Result	Evidence type
Operating domain	Design supply range	3.5-6.0 V	Design specification
Operating domain	Frequency range	100-800 kHz	Schematic simulation
Operating domain	Fixed frequencies	250 and 500 kHz	Schematic simulation
Reference	Temperature coefficient	15.67 ppm/°C	Schematic simulation
Reference	Low-frequency PSR	93 dB	Schematic simulation
LDO	Phase margin	62.492°	Schematic simulation
LDO	Load regulation	0.225 mV/mA	Schematic simulation
LDO	Line regulation	0.166%/V	Schematic simulation
Oscillator	Supply-related frequency span	0.3125%	3.6-6.0 V sweep
Oscillator	Temperature-related frequency span	0.28575%	-40 to 125 °C sweep
Oscillator	Power at 500 kHz	532 µW	5 V, TT, 25 °C

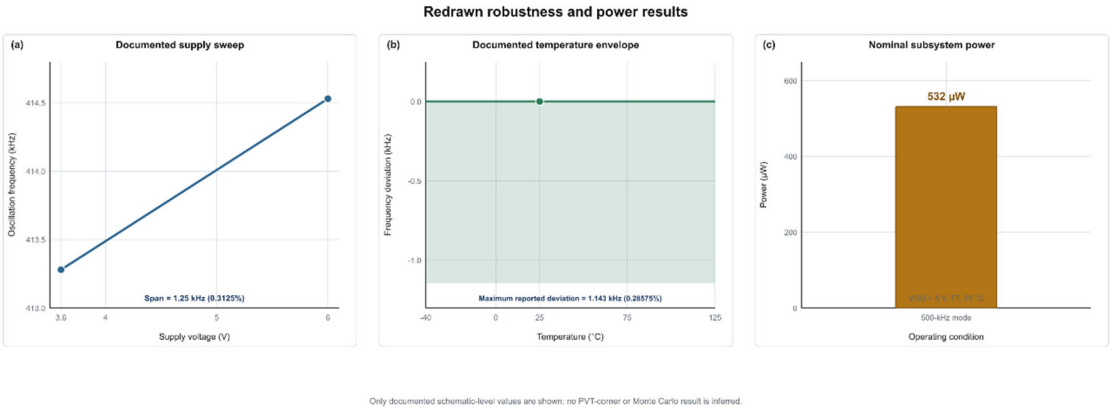


Fig. 6 Redrawn robustness and power results: (a) documented supply sweep, (b) documented temperature envelope, and (c) nominal subsystem power. Only documented schematic-level values are shown; no PVT-corner or Monte Carlo result is inferred.

5.4. Interpretation of the Integrated Results

The support-block and oscillator results are mutually consistent but should not be combined into a stronger claim than the data permit. High low-frequency rejection in the reference and regulator reduces the gain from the input rail to the charging current, while the remaining frequency span includes threshold, bias, and delay effects that are not separated by the present sweeps. The 0.3125% supply-related span therefore characterizes the integrated schematic under the documented programmable-mode condition; it is not a measured line-sensitivity guarantee for every mode.

Similarly, the 0.28575% temperature-related span is an end-to-end result rather than a direct measure of the reference temperature coefficient. The reference, resistor, current mirrors, comparators, and latch can have different curvature and partially offset one another over a finite range. Reporting both the 15.67-ppm/°C reference result and the oscillator's total frequency span exposes that distinction and avoids attributing system stability to a single block. Additional raw sweep points would be required for curvature analysis or a statistically meaningful worst-case model.

6. Discussion

6.1. Comparison with Prior RC Oscillators

Table 5 places the simulated design beside representative measured RC oscillators and timers. The comparison must be interpreted cautiously: the cited designs optimize frequency reference performance and report silicon measurements, whereas the present work reports a wider-input, multi-mode DC-DC support subsystem at schematic level. The proposed design does not lead the power-efficiency or temperature-coefficient metrics. Its distinguishing features are the 3.5-6.0-V integration target, four practical frequency-control paths, and a co-designed reference and regulator in a mature 0.18-µm process.

Table 5. Comparison with representative integrated RC frequency references.

Work	CMOS	Frequency	Power or efficiency	Stability indicator	Validation
Lu and Liao [2]	0.18 µm	8.2 MHz	46.3 µW	123 ppm/°C	Measured
Khashaba et al. [3]	65 nm	32 MHz	34 µW	8.4 ppm/°C	Measured
Park et al. [4]	65 nm	100 MHz	1 µW/MHz	±140 ppm, -40 to 95 °C	Measured
Zhao et al. [5]	0.18 µm	1 kHz-1 MHz variants	2.7 nW/kHz at 100 kHz	82 ppm/°C at 1 MHz	Measured
Jung et al. [6]	Reported CMOS	32.7 kHz	1.08 nW/kHz	13.2 ppm/°C	Measured
This work	0.18 µm	100-800 kHz	532 µW at 500 kHz	0.28575% total sweep	Schematic simulation

The comparison also explains the power result. Advanced wake-up timers operate from low supplies and aggressively duty-cycle or power-gate their analog blocks [5, 6]. The present subsystem maintains a wide-input regulator, reference, multiple bias branches, mode decoding, ramp generation, and protection-related support. Its 532-µW nominal result is therefore a system-level integration tradeoff rather than a direct competitor to sub-microwatt timers. If lower standby power becomes the primary requirement, the architecture can be extended with mode-dependent bias scaling or self-synchronized power gating, but those changes require new startup and transient verification.

6.2. Limitations and Required Next Steps

The strongest limitation is the absence of silicon data. Schematic simulation cannot capture package stress, unmodeled substrate coupling, parasitic asymmetry, fuse-programming spread, or measurement-interface loading. The absence of Monte Carlo and process-corner results also prevents a production-yield claim. Frequency variation is reported as the span present in the available sweeps and should not be interpreted as a guaranteed production limit. Similarly, external-clock operation requires dedicated lock-range and phase-error tests before it can be described as accurate synchronization.

A complete qualification sequence should begin with extracted-layout simulations at all operating modes, followed by process-voltage-temperature corners and mismatch Monte Carlo analysis. Startup time, duty ratio, cycle-to-cycle jitter, phase noise, and load-step sensitivity should then be characterized. After fabrication, the same matrix should be repeated across multiple dies and temperatures, with pre-trim and post-trim distributions reported separately. These steps would convert the current design paper into a measurement-backed frequency-reference study and clarify whether the support-block power can be reduced without degrading wide-input robustness.

7. Conclusions

A multi-mode RC oscillator subsystem for DC-DC converters has been designed in a CSMC 0.18-μm 1P6M CMOS process. The architecture distributes accuracy requirements across a supply-rejection-enhanced reference, a compensated local regulator, a low-drift bias and trim network, mode-controlled charging currents, and an alternating-capacitor relaxation core. It supports nominal 250- and 500-kHz fixed modes, resistor-programmed operation from 100 to 800 kHz, and an external-clock functional path.

Schematic-level results show a reference temperature coefficient of 15.67 ppm/°C, 93-dB low-frequency reference PSR, a 62.492° LDO phase margin, 0.3125% frequency span over the documented 3.6-6.0-V sweep, and 0.28575% span over the documented -40 to 125 °C sweep. Nominal subsystem power is 532 μW at 500 kHz. These results support the feasibility of the integrated architecture while also defining the remaining work: extracted-layout simulation, corner and mismatch analysis, external-synchronization characterization, and silicon measurement.

References

[1] Razavi, B. (2021). The design of a low-voltage bandgap reference [The Analog Mind]. IEEE Solid-State Circuits Magazine, 13(3), 6-16. https://doi.org/10.1109/MSSC.2021.3088963

[2] Lu, S.-Y., & Liao, Y.-T. (2019). A low-power, differential relaxation oscillator with the self-threshold-tracking and swing-boosting techniques in 0.18-μm CMOS. IEEE Journal of Solid-State Circuits, 54(2), 392-402. https://doi.org/10.1109/JSSC.2018.2877927

[3] Khashaba, A., Zhu, J., Pal, N., Ahmed, M. G., & Hanumolu, P. K. (2022). A 32-MHz, 34-μW temperature-compensated RC oscillator using pulse density modulated resistors. IEEE Journal of Solid-State Circuits, 57(5), 1470-1479. https://doi.org/10.1109/JSSC.2021.3121014

[4] Park, K.-S., Khashaba, A., Abdelrahman, A., Li, Y., Wang, T., Xia, R., Pal, N., & Hanumolu, P. K. (2023). A 1-μW/MHz RC oscillator with three-point trimmed 2.1-ppm/°C and single-point trimmed 8.7-ppm/°C stability from -40 °C to 95 °C. IEEE Journal of Solid-State Circuits, 58(7), 2064-2074. https://doi.org/10.1109/JSSC.2022.3227191

[5] Zhao, G., Xiao, Z., Mak, P.-I., Martins, R. P., & Law, M.-K. (2024). One-cycle-startup relaxation oscillator using ratiometric threshold-referenced and self-synchronized power gating techniques. IEEE Transactions on Circuits and Systems II: Express Briefs, 71(1), 56-60. https://doi.org/10.1109/TCSII.2023.3295269

[6] Jung, J., Kim, I.-H., Kim, S.-J., Lee, Y., & Chun, J.-H. (2018). A 1.08-nW/kHz 13.2-ppm/°C self-biased timer using temperature-insensitive resistive current. IEEE Journal of Solid-State Circuits, 53(8), 2311-2318. https://doi.org/10.1109/JSSC.2018.2824307

[7] Zhang, G., Yayama, K., Katsushima, A., & Miki, T. (2018). A 3.2 ppm/°C second-order temperature compensated CMOS on-chip oscillator using voltage ratio adjusting technique. IEEE Journal of Solid-State Circuits, 53(4), 1184-1191. https://doi.org/10.1109/JSSC.2017.2772808

[8] Peng, H., Lin, H., Chai, Z., Zheng, Z., & Peng, J. (2022). Design of a bandgap reference with low temperature drift and high PSRR. In Proceedings of the 2022 IEEE 4th International Conference on Circuits and Systems (ICCS) (pp. 180-186). IEEE. https://doi.org/10.1109/ICCS56666.2022.9936160

[9] Liu, N., Agarwala, R., Dissanayake, A., Truesdell, D. S., Kamineni, S., & Calhoun, B. H. (2019). A 2.5 ppm/°C 1.05-MHz relaxation oscillator with dynamic frequency-error compensation and fast start-up time. IEEE Journal of Solid-State Circuits, 54(7), 1952-1959. https://doi.org/10.1109/JSSC.2019.2911208