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A Review of Wearable EC System Design and Key Technologies

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Abstract: Wearable electrocardiogram (ECG) monitoring has attracted increasing attention as cardiovascular diseases remain a major global health concern and long-term physiological monitoring is shifting from clinical settings to daily life. Despite recent advances in wearable healthcare technologies, reliable and low-power ECG acquisition remains challenging due to the low amplitude of biopotential signals, motion-induced artifacts, common-mode interference, and strict energy constraints. Many existing studies focus on individual components, such as electrodes, analog front-ends, or wireless communication modules, while system-level interactions and design trade-offs are less frequently addressed. This paper reviews the key engineering considerations involved in wearable ECG system design from a system-level perspective. The discussion covers the characteristics of ECG biopotentials and the evolution of electrode technologies, weak-signal acquisition and conditioning techniques in analog front-ends, Σ-Δ analog-to-digital conversion for narrow-band ECG signals, and commonly used wireless communication approaches for long-term monitoring. In addition, architectural trade-offs between distributed and integrated hardware implementations are discussed. Overall, this review aims to provide a coherent overview of how different design choices jointly influence performance, robustness, and energy efficiency in wearable ECG systems.

Keywords: Wearable electrocardiogram; Bioelectric signal acquisition; Analog front end; Σ-Δ analog-to-digital converter; Wireless communication.

1. Introduction

In recent years, with the rapid development of wearable technologies, flexible electronics, and intelligent healthcare systems, this traditional clinical monitoring approach has gradually expanded from hospital settings to home-based environments, sports applications, and long-term chronic disease management. According to global mortality surveillance data released by the World Health Organization, cardiovascular diseases have remained the leading cause of death worldwide since 2000. In 2022 alone, they resulted in approximately 19.8 million deaths, accounting for about one third of all global deaths [1]. Therefore, early identification of arrhythmias, ischemic diseases, and long-term changes in cardiac function is of critical importance for reducing mortality. Compared with traditional short-term clinical examinations, continuous, non-invasive, and real-time surface electrocardiogram monitoring can provide richer dynamic physiological information, offering clinicians valuable evidence for clinical decision-making and supporting early risk warning as well as timely responses to acute events [2]. Thus, designing wearable ECG monitoring systems with high signal fidelity, improved wearing comfort, low power consumption, and strong portability has emerged as a key research focus in biomedical engineering and embedded systems in recent years.

Conventional wired ECG machines, like Holter monitors, are popular due to their ability to record stable ECGs and their familiarity to clinicians [3]. However, they are inconvenient for use outside the medical setting for an extended period. The device is cumbersome to handle. The wires are prone to tangling and breaking. Normal daily activities tend to interfere with the equipment. In wearable ECG applications, the electrodes are placed on the skin, and the data is sent wirelessly using low-power components. They are easier to wear for a long period and can be used at home or during physical exercise. In such applications, the acquisition of the signal becomes more challenging. The skin and electrodes do not have a constant contact; the impedance is high and can also vary with time. Motion can also affect the contact and cause artifacts. The surface ECG signal itself is a small signal with low frequency (millivolt level), and hence it is susceptible to power-line noise, muscle activity, and electromagnetic coupling from other devices.

Based on the above background, this paper provides a systematic review of the key modules in wearable ECG systems. Section 2 introduces the characteristics of bioelectrical signals and the evolution of electrode materials, and clarifies the decisive role of interface stability in signal fidelity. Section 3 presents wearable ECG hardware architectures and representative implementation pathways, and compares the engineering characteristics of distributed and integrated solutions. Section 4 analyzes the core modules of wearable ECG devices, including analog front ends, Sigma-Delta (Σ-Δ) analog-to-digital converters, digital signal processing, and wireless communication. The aim of this work is to clarify the key technical logic of the wearable ECG signal chain, summarize the design considerations and evolution trends of each module, and provide engineering references for high-fidelity, low-power, and long-term ECG monitoring.

2. Bioelectric Signal Acquisition and Conditioning

2.1. Bioelectric Signals and Electrode Materials

ECG biopotentials are millivolt-level signals measured using surface electrodes. In biomedical and wearable devices, the signal of interest typically lies in the low-frequency band of 0.05-150 Hz [4]. The ST-T region is especially dependent on accurate low-frequency acquisition; therefore, the front-end circuit must preserve near-DC and ultra-low-frequency components. In wearable devices, electrode inputs are exposed to large common-mode disturbances, slow baseline drift, and DC offset. As a result, ECG monitoring requires simultaneous handling of low signal levels, narrow bandwidth, and large common-mode interference. The electrode-skin interface is not an ideal contact; instead, it is a frequency-dependent network consisting of stratum corneum resistance, body fluid resistance, and double-layer capacitance. Relative motion between the electrode and skin changes the equivalent impedance and polarization voltage, which modulates the ECG waveform and introduces baseline drift and morphological distortion. Therefore, practical ECG monitoring depends on stable low-frequency coupling, motion-artifact suppression, and signal-fidelity preservation under strong common-mode interference.

2.2. Requirements of electrodes for bioelectrical signals and the evolution of electrode materials

Because of the characteristics of bioelectrical signals and the interference environment, electrodes in the ECG signal chain do more than introduce the signal. Their interfacial stability directly affects low-frequency fidelity and motion-artifact suppression. Under this constraint, electrode materials for wearable ECG systems have evolved through three major generations.

2.2.1. Ag/AgCl gel wet electrode

First-generation wet electrodes were chosen as the initial point because the electrolyte gel can fill micro-wrinkles on the skin and create ionic conduction pathways. Therefore, they can sustain a relatively low interfacial impedance even at 0.05 Hz, which makes it possible to preserve the low-frequency morphology of the ST-T segment. This generation set the paradigm of low impedance and low polarization. However, they have disadvantages in terms of dehydration of the electrolyte gel, skin irritation, and the use of disposable consumables during long-term use. These disadvantages have been pointed out in the criticisms of wet-electrode applications [5].

2.2.2. Dry contact electrode

Because gel-based wet electrodes have limitations, second-generation transitional electrodes remove the need for electrolyte gel. These electrodes include metallic or conductive-rubber dry electrodes, textile electrodes such as silver-coated knitted fabrics, and capacitive electrodes that transmit surface potentials through a thin dielectric layer. Dry-contact and non-contact electrodes generally present higher equivalent source impedance. They are more susceptible to displacement and sweating below 10 Hz; therefore, running and sweating can introduce baseline drift and superimposed power-line interference. These electrodes require front ends with higher input impedance and stronger artifact-rejection algorithms [6].

2.2.3. Flexible electronic skin electrodes

The concept of flexible skin electrodes came into being as a result of a structural paradigm shift in the instability problem related to the first two generations of electrodes when they are in motion. The use of flexible materials that are stretchable, bendable, and breathable enables these electrodes to move along with the skin. This is a way of achieving mechanical stability to translate into electrical stability at both the material and structural levels. The flexible skin electrodes are more stable than the conventional dry electrodes in terms of electrode–skin contact.

2.3. System-Level Functional Framework

As illustrated in Figure 1, a wearable ECG solution typically involves a multi-step signal chain consisting of electrodes, an analog front end (AFE), an analog-to-digital converter (ADC), a digital processing unit, a wireless communication module, and a mobile terminal or cloud server. The AFE provides signal gain, common-mode rejection, and input bias control before digitization. The signal is then converted into digital form by a high-resolution Σ-Δ ADC and transmitted to an MCU or a tailored ASIC for further processing [7][8]. After QRS-complex detection, heart-rhythm analysis, and data compression, the digital processing unit transmits the information to a smartphone client or hospital cloud server through low-power wireless communication such as BLE or Wi-Fi, enabling real-time ECG waveform display and event notification [8].

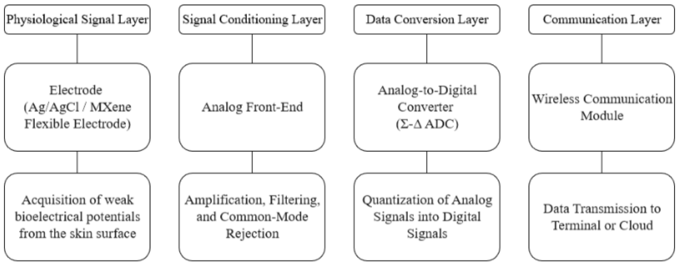

Figure 1. System architecture of a wearable ECG monitoring device

2.4. Typical Hardware Structures

As shown in Figure 2, the hardware components of wearable ECG systems can be implemented using two design approaches: distributed architectures and integrated architectures. In a distributed architecture, the system is divided into separate modules, including an analog front end (AFE), an analog-to-digital converter (ADC), a microcontroller unit (MCU), and a wireless transceiver. This modular structure supports fast prototyping, easy component replacement, and algorithm development without rebuilding the entire system. However, the system becomes more complex at the board level. Interconnects among analog, digital, and RF domains introduce parasitic effects, so power integrity, grounding, shielding, and driver-loop stability require detailed layout work and bench testing. A common distributed architecture uses a dedicated ECG AFE chip such as the ADS1292R. This chip includes a 24-bit Σ-Δ modulator, lead-off detection, and respiration-impedance measurement, and it can interface with high-impedance electrodes without major changes to the communication stack or firmware organization. These advantages explain why distributed architectures remain widely used in system exploration and algorithm development [9].

In contrast, an integrated architecture is a highly integrated architecture of the AFE, ADC, processing unit, and wireless communication on a single chip or system-in-package (SoC/SiP). The key features of this architecture include minimized signal routes, significantly reduced parasitic capacitance and inductance, and effective suppression of cross-domain coupling. Clocking and power management are also more centralized, providing outstanding performance in terms of area, power, and device-to-device variability. This architecture is typically used in mass-produced form factors such as chest patches and smartwatches. One representative product is the MAX30003, which combines high input impedance, EMI rejection, DC lead-off detection, and low-power standby and wake-up capability in a single chip. It has the capability to drive data streams for heart rate analysis and waveform processing directly and can be used in combination with a low-power BLE solution or an SoC solution to provide continuous monitoring in a compact form factor. The major strengths of this architecture are low power and ease of compliance, and the major weakness is low flexibility with a limited space for low-level parameter modification.

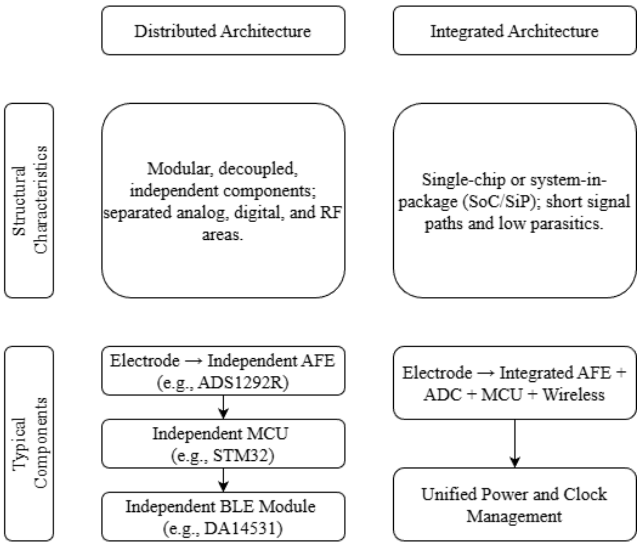

Figure 2. Comparison of distributed and integrated architectures

Overall, distributed architectures are well suited to early R&D stages where component interchangeability, fast algorithm iteration, and experimental flexibility are emphasized. Integrated architectures are more appropriate for productization, where low power, miniaturization, and manufacturing consistency are prioritized. The two approaches are not mutually exclusive. Instead, they play complementary roles at different stages of development and jointly support the evolution of wearable ECG systems.

3. Key Modules

This chapter discusses four main modules in wearable ECG devices: the analog front end, analog-to-digital conversion, digital signal processing, and wireless communication. The discussion focuses on their roles in signal quality, power consumption, and system-level design.

3.1. AFE

The analog front-end (AFE) represents the first stage of a wearable ECG system. Its primary function is to detect the μV-level biopotentials gathered through skin electrodes and prepare the signal for conversion into the digital domain. The instrumentation amplifier is the most critical in all the components, as it determines whether the signal can be accurately digitized for diagnostic use. ECG signals are inherently weak, have high source impedance, and are often affected by strong common-mode signals. It makes strict demands on the front-end circuitry in terms of input impedance, common-mode rejection, and baseline stability. However, due to limitations in device matching and drift, amplifier circuits often prove insufficient for acquiring diagnostic-quality ECG signals.

Instrumentation amplifiers address these shortcomings at the architectural level through a symmetric differential architecture, high-input-impedance buffering stages, and a well-matched resistor network. The basic concept is to amplify the difference between the two input signals, which preserves the differential signal while canceling out the common-mode signal. The input buffer stage provides a very high input impedance to avoid loading the electrode interface. The above differential amplification stage and the use of precision-matched resistors make it possible to achieve a high CMRR, thus effectively eliminating common-mode interference. This circuit is designed to process very weak signals even in the presence of strong common-mode noise, providing a solid foundation for reliable, high-quality signal performance in ECG front-end systems.

In industrial practice, the three-op-amp instrumentation amplifier has long been a mainstream solution. Its internal structure typically comprises an input buffer stage, an intermediate differential gain stage, and an output buffer, achieving a balanced trade-off between high input impedance and common-mode rejection. Due to its maturity and energy efficiency, this architecture is widely adopted in portable and wearable devices. A representative implementation is Texas Instruments' ADS129x series, which consolidates key analog and digital modules on a single chip. By integrating a Σ-Δ ADC and a programmable gain amplifier on-chip, these devices significantly reduce sensitivity to parasitics and mismatches introduced by external interconnections, thereby improving system-level consistency and interference robustness. In addition, integrated lead-off detection and, in some variants, respiration impedance measurement allow auxiliary functions required for ECG monitoring to be implemented at the chip level, reducing peripheral circuit complexity. Taking the ADS1292R as an example, with appropriate system design it can achieve a CMRR exceeding 100 dB over a 150 Hz bandwidth. In two-channel mode, it offers an input-referred noise of approximately 8 μVpp (G = 6), while maintaining per-channel power consumption at the hundreds-of-microwatts level. It also supports sampling rates up to 8 kSPS to cover diagnostic ECG bandwidth requirements [9]. This integration-centered approach has made the ADS129x family a popular choice for portable and wearable ECG systems. It decreases the size of the PCBs and the number of components, as well as making the overall system more robust. However, the degree of integration is so high that it makes it difficult to design the front-end gain and interfaces, as there are a number of parameters that have to be fixed at an early stage of the design. This means that there is a trade-off between having a smaller design and being able to debug the system.

Scientific literature sometimes mentions chopper-stabilized and auto-zero amplifiers. The principle of operation of these amplifiers is to suppress 1/f noise and input offset by modulation and demodulation, in order to achieve improved low-frequency baseline stability. This type of circuit is normally studied in literature as a way to approach the limit of performance, but with more complex circuits. Switching activities can introduce transient effects and more demanding stability and power control.

In recent years, three-op-amp instrumentation amplifiers and their integrated ADC solutions have continued to improve in terms of noise, offset, and power consumption. Input noise density has been reduced to the tens of nV/√Hz range, input offset voltage has been controlled within tens of μV, and per-channel power can be lowered to the hundreds-of-μW level.

These advances have strengthened the feasibility of long-term, low-power ECG monitoring in wearable scenarios. Nevertheless, bottlenecks remain. The coupled trade-offs among power, bandwidth, and noise limit further improvements. Electrode bias drift is difficult to fully compensate due to fluctuations in skin-contact impedance. Maintaining ultra-high input impedance while reducing chip area and controlling leakage currents still requires careful compromises between process technology and circuit design.

3.2. ADC

The analog-to-digital converter links the analog front-end section and the digital signal processing section. Its role is to translate a continuous-time voltage signal into discrete digital codes, so it strongly influences digital-domain signal quality. A general ADC structure includes a sample-and-hold circuit, a quantizer, and an encoder, and can also include a modulator and digital filtering. Among ADC architectures, Sigma-Delta (Σ-Δ) converters are widely used in ECG systems. A Σ-Δ ADC typically includes an integrator, a quantizer, and a feedback loop. The integrator accumulates the difference between the input and the feedback signal. The quantizer performs coarse conversion using either 1-bit or multi-bit quantization. The feedback loop completes the feedback path and determines noise shaping. Most quantization noise is shifted to higher frequencies, leaving lower in-band noise within the ECG frequency range. Oversampling further decreases the noise density in the ECG band. Because ECG is a narrow-band signal ranging from approximately 0.05 to 150 Hz, oversampling and noise shaping improve the effective number of bits in the low-frequency region. A decimation filter, such as a CIC or FIR filter, removes high-frequency noise and reduces the sampling rate to 250-500 SPS. Digital notch filtering at 50/60 Hz can then be implemented efficiently.

The ADS1292R from Texas Instruments is a representative implementation of a Σ-Δ modulator for wearable ECG. Beyond serving as a component example, it demonstrates how the Σ-Δ conversion method can be integrated into a robust system design. The chip contains a Σ-Δ modulator, a programmable gain amplifier (PGA), a right-leg drive (RLD), and a lead-off detection function. This integration preserves converter-level noise shaping while also improving system-level robustness.

From an architectural standpoint, the ADS1292R follows a conventional Σ-Δ conversion process. Oversampling is central to this design. The data rate is programmable from 125 SPS to 8 kSPS, and the Σ-Δ modulator operates well above the Nyquist rate, spreading quantization noise over a wider bandwidth. A noise-shaping feedback loop shifts much of this quantization noise into higher-frequency bands, reducing noise within the ECG band of interest (0.05-150 Hz). Consequently, the device provides approximately 8 μVpp input-referred noise at a gain of 6 with a 150 Hz bandwidth [9]. A digital decimation stage then suppresses out-of-band quantization noise and reduces the sampling rate to the level needed for processing, usually 250-500 SPS. The PGA adjusts gain so that the electrode signal remains within the modulator input range: small signals are not buried in noise, and large input signals do not overload the converter. The RLD and lead-off functions improve stability when electrode impedance is high by rejecting common-mode noise and detecting electrode contact. High integration density also shortens analog signal paths and reduces mismatches and parasitic effects from external interconnects. For diagnostic ECG, the lower bandwidth limit helps retain ST-segment and repolarization information, while the upper bandwidth limit preserves QRS time-domain information [4].

3.3. Digital Signal Processing

Digital signal processing (DSP) is the stage that converts digitized ECG samples into clinically and operationally useful information. After ADC conversion, the raw ECG stream still contains residual baseline wander, power-line interference, motion artifacts, and muscle noise. DSP therefore performs filtering, segmentation, feature extraction, rhythm analysis, and data compression. A typical wearable ECG pipeline includes a high-pass filter for baseline-wander suppression, a low-pass or band-pass filter for noise reduction, a 50/60 Hz notch filter for power-line interference, and QRS-complex detection for beat localization. Reliable QRS detection is especially important because heart-rate estimation, rhythm classification, and event-triggered wireless transmission depend on accurate R-peak timing.

In wearable systems, DSP design is constrained by memory, computation, latency, and power. Lightweight filters and rule-based QRS detectors are often preferred for always-on operation because they can run on low-power MCUs with predictable execution time. More complex algorithms can improve robustness under motion and poor electrode contact, but they increase computational load and battery consumption. A practical design therefore balances algorithmic accuracy with energy efficiency by combining local preprocessing, adaptive thresholding, data compression, and event-driven transmission. In this system-level context, DSP also links the ADC and wireless modules: better filtering and compression reduce the amount of data that must be transmitted, while reliable event detection allows the wireless module to remain in a low-duty-cycle state during normal monitoring.

3.4. Wireless Communication

Wireless communication determines how ECG information is transmitted from the body and how much energy is required for this transmission. In wearable ECG systems, common options include BLE, low-power Wi-Fi, and cellular IoT. For short-range communication, BLE typically uses a smartphone or tablet as a gateway. Its advantages include native compatibility with mobile devices and low connection current, while its bandwidth is sufficient for single- or multi-lead ECG streaming at 250-500 SPS [10][11][12][13][14]. Wi-Fi is suitable for hospital-wide coverage or bandwidth-intensive use cases, although traditional 802.11n/ac can be difficult to use in small battery-powered form factors. Low-power Wi-Fi solutions such as IEEE 802.11ah and 802.11ba Wake-Up Radio reduce idle power consumption through narrowband operation, long sleep cycles, range extension, or a secondary wake-up radio [15]. For remote monitoring independent of a smartphone, cellular IoT technologies such as LTE-M and NB-IoT provide direct wide-area connectivity. NB-IoT supports low-power small-message reporting through repeated transmission, whereas LTE-M provides lower latency and higher data rates. Battery life mainly depends on PSM/eDRX control and uplink reporting intervals. In practice, wearable ECG systems often combine local buffering with event-driven transmission so that idle connectivity remains low duty cycle while critical events receive higher bandwidth.

4. Conclusion

Existing research shows that, although substantial progress has been achieved in signal acquisition, processing, and transmission, wearable ECG systems still require careful trade-offs among signal quality, energy consumption, wearing comfort, and system reliability in real-world settings. This review provides a system-level overview of wearable ECG design. From this perspective, the functional components discussed above do not operate in isolation; instead, they interact across the electrode interface, analog front end, ADC, DSP algorithms, wireless link, and power-management strategy. The development of wearable ECG monitors is shifting from isolated component optimization toward integrated system design, with growing attention to interface stability, hardware integration, energy-aware operation, and responsible use of physiological data. This paper focuses mainly on hardware-centric system design and therefore does not provide an in-depth analysis of software-layer optimization or clinical algorithm validation. With continuing progress in flexible electronics, low-power integrated circuits, wireless communication, and signal processing, wearable ECG monitoring systems are expected to become more mature and usable, supporting more reliable long-term cardiac monitoring in real-world healthcare settings.

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