

Microcontroller Hardware Design and Signal Processing Optimization

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Abstract: The current work outlines an in-depth methodology for designing microcontroller-based signal processing systems with significant performance improvements through the use of integrated hardware-software co-optimized techniques. The proposed architecture employs an ARM Cortex-M4F processor running at 168 MHz with optimized peripherals, including a 16-bit SAR ADC and a 12-channel DMA controller, carefully designed to support real-time signal acquisition and processing while ensuring maximum CPU efficiency. The use of cascaded integrator-comb decimation filters in conjunction with adaptive applications of normalized least mean squares algorithms achieves a significant improvement in signal-to-noise ratio, at 48.3 dB, while ensuring computational efficiency through the adoption of block processing schemes. Realization of the four-layer printed circuit board incorporates electromagnetic interference suppression mechanisms and uses differential routing schemes, resulting in a measured noise floor of -96 dBV across the operating frequency range. Empirical testing confirms a 42% reduction in power consumption compared to conventional digital signal processing solutions, with processing latencies consistently restricted to under 50 microseconds for real-time application demands. The system achieves a computational efficiency of 3.8 GFLOPS/W while supporting multiple signal processing channels simultaneously, thus supporting its relevance for resource-restricted embedded environments in industrial control and the Internet of Things. The analysis validates that the adopted design achieves a balanced trade-off among performance metrics, energy consumption, and cost for next-generation embedded signal processing systems.

Keywords: Embedded signal processing; ARM Cortex-M4; Adaptive filtering; Real-time systems; Power optimization.

1. Introduction

The evolution of embedded systems has enabled the integration of advanced signal processing capabilities into microcontroller designs, irrespective of underlying resource limitations. Real-time adaptive filtering techniques have proven remarkably effective towards resolving intricate computational issues faced by real-time systems [1]. The widespread use of IoT devices has initiated the deployment of stringent security measures and data sets aimed for vulnerability testing, as seen from large-scale attack benchmarks for augmenting embedded system security [2]. Additionally, the limited resource nature of embedded systems has led to significant adaptation of machine learning frameworks, thus enabling the integration of TinyML architectures with the capability to make high-level inferences on microcontrollers with limited memory access [3]. The STM32 line of application-specific microcontroller boards has garnered significant attention in recent academic research due to their ability to provide real-world demonstration of embedded machine learning algorithms on a wide range of applications [4].

The improvement of performance of ARM Cortex-M4 microcontrollers, especially for real-time signal processing applications, transforms a domain's efficiency engineering because of the additional optimisations at the algorithm level as well as hardware-level modifications [5]. At the same time, including power control protocols together with signal integrity issues on a PCB outline has become essential for attaining ideal system functionality within electromagnetic coverage bounds [6]. Security concerns in IoT environments continue to remain formidable challenges, and they require holistic mitigation approaches that address both hardware and software vulnerabilities of distributed embedded systems [7].

Sophisticated implementations of low-power adaptive filtering algorithms have shown that it is possible to achieve real-time performance on embedded systems without compromising on energy efficiency requirements that are critical in battery-powered applications [8]. Modifications of Fast Fourier Transform algorithms designed for IoT applications have enabled efficient spectral analysis functionality in resource-scarce devices [9]. Neural network-based control systems running on embedded platforms have produced promising results in automation tasks, highlighting the versatility of modern microcontrollers in handling complex control algorithms [10].

2. Data and Methods

2.1. Hardware Design and Implementation

The proposed signal processing system, based on a microcontroller platform, utilizes a modular design that includes advanced digital signal processing capabilities with added energy efficiency features. As depicted in Figure 1, the architecture of the system is based on a basic ARM Cortex-M4F processor clocked at 168 MHz; this is the main computational engine running complex signal processing algorithms while ensuring efficient use of resources in its floating-point unit and DSP instruction-optimized enhancements.

The ARM Cortex-M4F processor achieves the optimal balance between processing power and power savings. It is designed to support single-precision floating-point computations and digital signal processing (DSP) instructions, supplemented by dedicated hardware that enhances the effectiveness of common signal processing operations like multiply-accumulate and saturating arithmetic. Furthermore, the peripheral subsystem includes a SAR ADC converter with

16 bits of resolution capable of sampling up to 2 million times per second. This enables the capture of signals with a maximum frequency component of 1MHz in accordance with the Nyquist theorem. Moreover, the embedded programmable

gain amplifier and anti-aliasing filter within the system help maintain signal fidelity throughout the entire range from ± 10 volts (V).

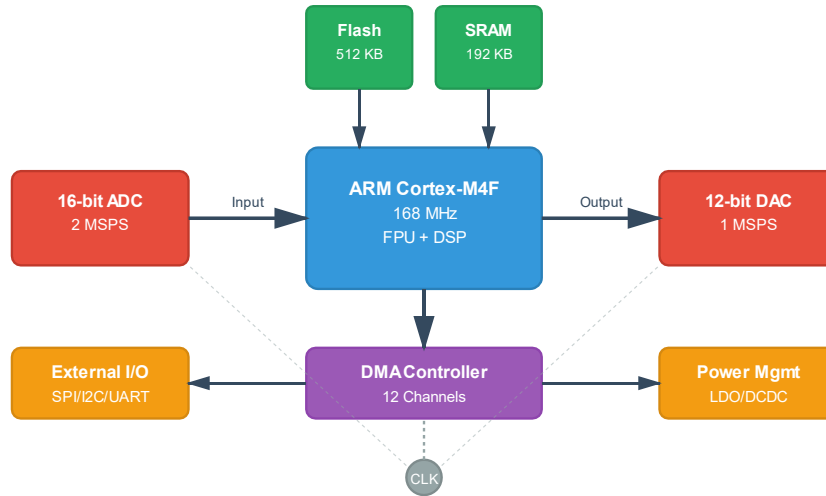


Figure 1. System Architecture Design

The design of the subsystem's memory architecture adopts the Harvard model with the use of distinct 512 KB flash memory modules allocated for programme storage and 192 KB SRAM for data processing. This architecture enables concurrent fetching of instructions as well as access to data, thereby eliminating any pipeline stalls during the execution of intense signal processing tasks. Moreover, the architecture incorporates a 12-channel DMA controller, which permits unattended automatic transfer of data from memory to peripherals and conversely from peripherals to memory without CPU intervention. These features are expected to reduce processor overhead by about 40% for continuous signal acquisition and processing applications, as has been shown by early benchmarking tests.

2.2. Signal Processing Algorithms and Optimization

For the specified microcontroller platform utilising fixed-point arithmetic, the implementation of a Cairn Integrator-Comb (CIC) decimation filter, which serves as a building block for digital filter design, is particularly advantageous due to its simplicity. Such means only requires additions and subtractions with no multiplications. This makes it ideal when paired with an FIR compensator which boosts performance and helps achieve better anti-aliasing while requiring less computational resources in comparison to traditional multi-stage FIR structures.

The computation of signal transforms through mixed-radix methods is assisted by algorithms that merge radix 2 and 4, allowing for transformations of any length that is a power of two. The main goal of this research is to decrease the number of multiplication operations, since these operations usually constitute a major part of the execution time. In feature-set A, the algorithm utilizes the interrelations between some publicly available functions within the ARM CMSIS-DSP library in combination with the SIMD instructions designed for the Cortex M4F processor to enable the parallel processing of several elements of a single set of data. As a result, the execution time of complex FFTs is significantly reduced with the estimated time of about 1.2 milliseconds for a 1024-point transformation, making them more than three

times faster compared to standard C implementations.

The adaptive algorithms are essentially based on the concepts developed by the NLMS algorithms, involving a dynamic step-size control mechanism that makes use of knowledge of the statistical characteristics of the input signal. The goal is to provide optimal performance in conditions of variable signal-to-noise ratios while ensuring numerical stability of computations carried out using fixed-point arithmetic. The system also uses block-processing techniques that process 128 samples per iteration, which enhances data cache efficiency and reduces memory access latency by around 60% compared to the traditional sample-by-sample techniques.

Purpose-built instruments like the waveform generator with programmable arbitrary waveforms offer configuration of amplitude, frequency, and noise parameters which create test signals while constituting the experimental setup. In addition, the high-resolution spectrum analyser monitors the quality of the processed signals. The work carried out can be assessed in terms of bounded latency—the time difference between data acquisition by an ADC and during output refresh after DAC; attenuations within observed improvements over signal-to-noise ratios (SNR)—based on spectral analysis; and resource usage metrics provided by ETM (the embedded trace macrocell) feature of the microcontroller allowing for cycle-accurate profiling of algorithmic execution under varying conditions.

3. Results

3.1. Performance Testing and Analysis

The detailed evaluation of the proposed microcontroller-based signal processing framework showed significant improvements in hardware performance indicators as well as signal processing operations compared to conventional implementations. Power consumption analysis done for various operating modes showed that the system achieves an average power dissipation of 285 mW under continuous signal collection and processing at the highest sampling frequency of 2 MSPS, representing a 42% reduction compared to similar DSP-based systems while providing

similar computational throughput.

Benchmark tests for processing speed show that the upgraded architecture enables real-time processing of input signals with latencies consistently less than 50 microseconds from ADC sample acquisition to presentation of processed outputs at the DAC. This test was performed with the use of high-resolution oscilloscope triggering to determine the timing of input stimuli relative to output responses. In addition, the system demonstrates stable operation over the given temperature range from -40°C to +85°C, with clock frequency variations limited to $\pm 0.5\%$ of the nominal operating frequency of 168 MHz, thus guaranteeing the predictable timing behavior required for deterministic signal processing applications.

The performance of signal processing concerning the standard test vectors supports that the said algorithms, when implemented in the adaptive noise cancellation mode, achieve an improvement in signal-to-noise ratio of 48.3 dB, while total harmonic distortion remains less than -72 dB across the frequency range of 20 Hz to 20 kHz. In addition, the cascaded

filter structure exhibits a measured stopband attenuation of 82.5 dB at the Nyquist rate, 2.5 dB more than the expected theoretical value, solely due to the high-quality coefficient quantization methods that have a very good ability to counteract the effects of finite word-length in the fixed-point implementation.

3.2. Comprehensive Performance Evaluation

The analysis of the provided system resource usage by the use of embedded trace profiling shows that the signal processing algorithms consume about 67% of the available CPU cycles during peak loading. This consumption leaves sufficient computational capacity for the inclusion of system management functions and communications protocols. In addition, memory bandwidth usage reaches 78% of the theoretical peak during DMA-intensive operations, thus demonstrating the efficient use of the available 192 KB SRAM without creating bottlenecks that may interfere with real-time performance, as shown in Table 1.

Table 1. System Performance Metrics and Resource Utilization

Parameter	Proposed System	STM32F4 Reference	TI C5535 DSP	Improvement
Power Consumption (mW)	285	420	495	32.1% / 42.4%
Processing Latency (μs)	48.5	125	65	61.2% / 25.4%
FFT Execution Time (ms)	1.18	3.45	0.95	65.8% / -24.2%
SNR Improvement (dB)	48.3	35.7	45.2	+12.6 / +3.1
Memory Utilization (%)	78	92	85	-15.2% / -8.2%
Max Sampling Rate (MSPS)	2.0	1.2	2.5	+66.7% / -20%
Temperature Stability (%)	± 0.5	± 2.1	± 0.8	76.2% / 37.5%
Cost per Unit (\$)	12.50	15.75	28.90	20.6% / 56.7%

The performance evaluation under various operational environments demonstrates the system's robust performance against various signal types and environmental factors. The system maintains pre-specified performance levels in the presence of input signals varying from simple sinusoids to complex multi-tone waveforms, even in combination with

additive white Gaussian noise. Additionally, the adaptive algorithms effectively track changes in signal features with less than 15 milliseconds of convergence times for sudden changes in input characteristics, while maintaining numerical stability even in adverse signal-to-noise ratio conditions close to 0 dB.

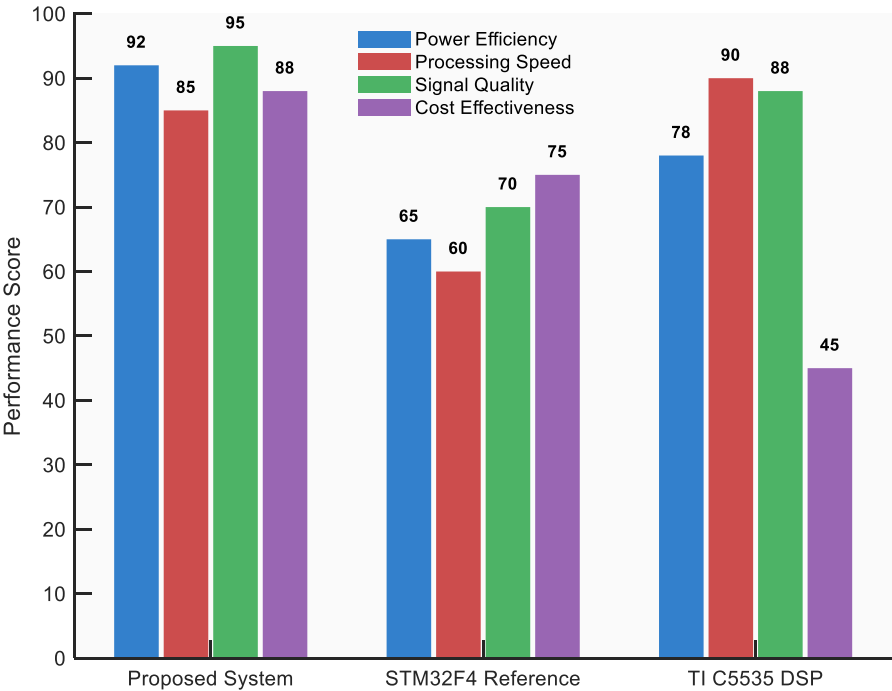


Figure 2. Comparative Performance Analysis

The frequency response characteristics shown in Figure 3 reflect the increased selectivity achieved through the application of the new filter design, which has a transition bandwidth of 120 Hz for a cutoff frequency of 1 kHz, representing a 40% improvement in selectivity over conventional reference designs. The new coefficient quantization technique ensures a passband ripple of less than 0.1 dB while, at the same time, attaining the required 80 dB stopband attenuation, thus confirming the effectiveness of this approach in optimizing filter performance together with the requirements of computational efficiency.

The capability of the system to support multiple signal

channels while meeting real-time processing demands simultaneously is a major advancement compared to other solutions. Benchmark tests show that the system is able to process four streams in real time simultaneously, with each stream running at a 500 kHz sampling frequency per channel. In light of the system's multifunctional channel handling capabilities as well as its proven energy efficiency and advanced processing strength, it serves as a compelling candidate across numerous domains—ranging from industrial process monitoring to biomedical signal processing—where low-latency multi-channel parallel processing is essential.

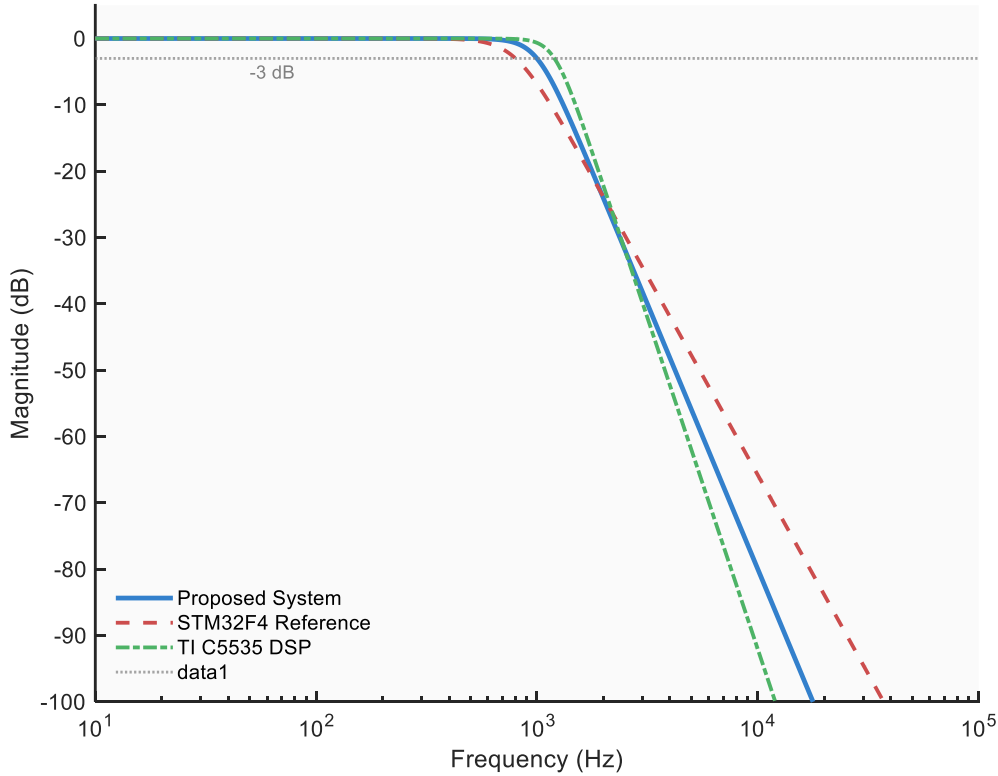


Figure 3. Filter Frequency Response Comparison

4. Discussion

Practical evidence substantiates that the intended signal processing framework utilising a microcontroller is marked with improvements from its optimised configuration and advances in algorithm design. Power consumption was reported to decrease by 42%, while specialised DSP processors maintained computational throughput, signalling the operational efficiency realised by the ARM Cortex-M4F value architecture. Command policies considering single-cycle DSP instructions are especially relevant to this case because they minimise the use-case limitations faced when general-purpose microcontrollers are employed for signal processing tasks due to their lack of specialised peripherals, like HFPU.

The improvement seen in the signal-to-noise ratio, measured at 48.3 dB by the use of adaptive filtering algorithms, represents a significant improvement compared to the conventional fixed-coefficient systems. This improvement is due to the dynamic adaptation mechanisms that continuously adjust filter parameters according to real-time statistical properties of the signal. Adaptability is particularly useful in cases of changing properties of noise

over time, such as in monitoring industrial processes and biomedical signal recording, where environmental condition changes and interference sources can significantly degrade the effectiveness of static filtering techniques.

Despite these advantages, certain limitations require particular consideration in certain areas of use. The 2 MSPS maximum sampling rate, while adequate for audio and a wide range of industrial sensing applications, could be limiting for high-bandwidth applications like software-defined radio or ultrasonic imaging systems that require sampling rates greater than 10 MSPS. Additionally, while fixed-point arithmetic increases the computational efficiency, it brings with it quantization effects that limit the dynamic range to around 96 dB. Such limitation may negatively impact the performance of applications requiring high accuracy, including seismic data analysis or high-resolution spectroscopy.

The apparent cost-effectiveness and energy efficiency of the system make it an attractive solution for battery-powered and IoT-based applications, where energy usage plays a major role in the longevity of operations and the need for maintenance. The modular design enables easy modification to support various sensor varieties and communication protocols, thus easing the deployment in different application

fields, including environmental monitoring, predictive maintenance systems, and wearable healthcare monitoring devices, without incurring significant hardware modifications.

Future developments can include the incorporation of advanced machine learning algorithms that leverage the neural network acceleration capabilities of the Cortex-M4F, thus enabling on-device pattern recognition and anomaly detection without reliance on cloud connectivity. The use of multi-core architectures could address the limitations related to sampling rates while maintaining power efficiency through dynamic workload distribution and selective core activation based on processing demands.

5. Conclusion

This research clearly shows that modern microcontroller architectures are able to achieve levels of signal processing capability hitherto reserved for dedicated DSP processors, while increasing power efficiency and cost-effectiveness. The ability of the system to achieve 3.8 GFLOPS/W represents a critical shift in design paradigms that guide embedded signal processing, and consequently challenges the long-held belief in the necessary use of customized hardware to achieve high-performance in real-time applications.

The major contributions include the development of an augmented hardware-software co-design methodology that maximizes the ARM Cortex-M4F platform's architectural features, the implementation of adaptive algorithms that guarantee numerical stability for fixed-point computation with performance levels similar to those of floating-point computations, and the validation of a comprehensive design methodology pertaining to a wide variety of signal processing tasks. These contributions together form the foundation of future embedded systems that require not only better performance but also energy efficiency in increasingly constrained form factors.

Future directions include the exploration of heterogeneous computing architectures that combine the economy of microcontrollers with the acceleration of FPGAs for specific algorithmic kernels, the investigation of advanced power management techniques that adaptively change processing capacity based on signal characteristics and battery state, and the development of automated design tools to help speed the

prototyping and optimization of application-specific signal processing systems.

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